# **EUROCHIP IN ACTION: A CASE STUDY**

ANTONIO DE BRITO FERRARI<sup>\*</sup>

This paper describes the experience of the Department of Electronics and Communications Engineering, Universidade de Aveiro, as a EUROCHIP Participating Institution (PI). The emphasis is on the analysis of the impact of EUROCHIP participation on the curricula of the degree courses run by the department. In a short time the curricula has changed from a traditional one, with no VLSI contents, to one where VLSI design is becoming a very strong presence. What has been achieved so far through EUROCHIP is described as well as the plans for the near future.

## 1. Introduction: Characterising the Department

The Department of Electronics and Communications Engineering of Universidade de Aveiro has been running a 5 year degree course in Electronics and Communications Engineering since 1974. The number of students has been increasing steadily since the mid 1980s, approaching 700 students enrolled in the course for the academic year 1991-92. In the present academic year an M.Sc. course in Electrical Engineering has started with 25 students attending it.

The Department has 42 academic staff, including 18 of professor rank (either Full Professors, Associate Professors or Assistant Professors), the others being Junior Lecturers, of which about 10 are on leave from teaching duties to do their Ph.D. research.

There are established research groups in Computer Architecture, with a strong interest in Parallel Architectures and VLSI implementations, Computer Networks, Biomedical Engineering, focusing on Biomedical Signal and Image Processing, Instrumentation, with instrumentation for Nuclear Physics as its main area of work, Microwaves and Optical and Digital Communications. Apart from the junior staff preparing a Ph.D., these groups support quite a large number of other Ph.D. students.

# 2. The Electronics and Communications Engineering Degree Program

## 2.1. The Curriculum in 1988

The last curriculum changes have taken place in 1984. The curriculum is the following:

in aliquity at issues it.

nah d

no la contragazione Programa della contragazione

\* Departamento de Electrónica e Telecomunicações, Universidade de Aveiro, 3800 Aveiro, Portugal

Carlord Sec.

£

Year Semester 1	Credits	Semester 2	Credits
1 Calculus I	4	Calculus II	4
Linear Algebra I	3.5	Linear Algebra II	3.5
Chemistry	4	Programming and Problem- Solving	4
English I	1.5	English II	1.5
2 Calculus III	4.5	Mathematics for Electrical Engineers	4.5
Numerical Analysis	3.5	Electromagnetic Waves	: 5
Probability and Statistics	3.5	Circuits and Signals I	4.5
Electromagnetism	.5	Introduction to Electronics	2
3 Circuits and Signals II	4.5	Modulation Theory II	4.5
Control Systems	4.5	Guided Propagation	4.5
Electronics I	4.5	Electronics II	4.5
Digital Systems	4	Computer Organisation	3.5
4 Antennas and Radiation	4.5	Communication Systems	3.5
	3.5	Instrumentation and Measurements	4.5
Digital Electronics	4.5	Non-Linear Control Systems	3
Operating Systems	4	Digital Signal Processing	3
and the second second		Electrical Machines	4
5 Project	7.5	Project	7.5
Technical Elective Al	4.5	Technical Elective B1	3
Technical Elective A2	4.5	Technical Elective B2	3
	en in inden in de ser in de se Tradicional de ser independent de s		3 .5
NOTE: Cradita include Laboratory work related to the course			• ***

NOTE: Credits include Laboratory work related to the course

The curriculum is a quite traditional one, as should be apparent from the list of courses, with an emphasis on transistor-level electronics courses mainly oriented towards analog electronics. The main changes in the curriculum prior to EUROCHIP participation have been the increase in the computing content of the degree program, although it still remains relatively weak when compared to the curricular in other countries that saw the increase in the computer contents of the curricula start much earlier than was the case in Portugal.

The most distinctive feature of this curriculum is its strong design orientation. Up to 1989 the main focus has been on electronic systems design based on off-the-shelf components, with students dedicating most of their final year, and a significant part of the preceding one, to electronic design. The designs they produce are fully tested and debugged, leading to working prototypes. Typically during their final year projects

32

students design a quite densely populated PCB based on off-the-shelf components and test and debug it, with two-layer printed circuit boards being produced within the department.

Various design tools have been used since the mid-80s: schematic capture packages (ORCAD, P-CAD, HP DCS) generating EDIF files and running on PCs and workstations are widely used. Placement and routing (HP PCDS accepting EDIF files as input) have been available on workstations. The introduction of the use of simulation tools, namely HILO and SPICE, also took place at the same time, although actual use was somewhat more restricted, due to the fact that topics on simulation have not been incorporated into the course programs, and hence students had to learn how to use them during their projects.

We believe the strong design orientation of the degree program is a distinctive characteristic among the Portuguese Electrical Engineering Schools and one of the main reasons for the strong market demand for our graduates.

## 2.2. First Efforts to Introduce VLSI

In the late 1980s it became apparent that electronic systems design based exclusively on off-the-shelf components was on the way to obsolescence. Hence the need to update the curriculum by providing the students with VLSI design capabilities was considered essential to keep the level of design expertise of our graduates.

In order to start that evolution in 1988 a joint proposal to FUNDETEC was put forward together with the Departments of Electrical Engineering of Oporto University and the Technical University of Lisbon (IST) for the funding of some VLSI design facilities. Funding was approved, with each Department receiving a colour workstation and a ES2 SOLO 1400 licence. Under the proposal the 3 departments should also try to develop a common program of studies in VLSI design.

Although modest this initiative allowed for the introduction in university degree programs in Portugal of industry-quality VLSI design tools. It was as well a quite innovative experience of collaboration between universities that were seeing themselves as having a common role to play in the modernisation of Electronic Engineering curricula in Portugal, rather than acting in the more traditional role of competitors trying to maximise their share of scarce funds. From the start it was actually apparent to them that this was a common mission that could only be carried out successfully through close cooperation among all those academics involved in VLSI design. This cooperation was later extended to the ESPRIT project "Special Action for Microelectronics in Portugal" (SAMPO), where the same people participate together with other, non-university, partners.

The availability of the SOLO design package was suitable to support student projects. It could also be used for a course on VLSI design if more seats were made available. However, being a Silicon Compiler system, it is not adequate to introduce a design on Silicon perspective on existing courses in the curriculum. Hence other VLSI design packages were needed, each with a reasonable number of licences, to be able to implement the changes we were seeking.

S VIN :

ŧ

and the provide states

## **3.** Participation in EUROCHIP

## 3.1. The Aims and the Requests

Shortly after the FUNDETEC initiative the call for proposals to a VLSI Design Action under the ESPRIT program was announced. In January 1989 the Department presented its case to become a member of the Action. The objectives were to be able to provide two different levels of expertise in VLSI design. The first level, general to all students, would provide a basic background in CMOS technology and some familiarity with design tools. The second level of expertise, to be achieved through final year Technical Elective courses and Project, would provide students with actual design experience, with students designing and testing VLSI chips and integrating them into larger systems.

To achieve the first goal the contents of the Electronics I and II and Digital Electronics courses would have to be changed. Concerning the latter, the first part of the course had traditionally concentrated on the analysis of the characteristics of the different logic families with particular emphasis on analysis at the circuit level. This is to be changed by concentrating on CMOS and taking a VLSI approach to it. The material to be covered will be similar to the Part I -Introduction to CMOS Technology of the Weste and Eshraghian book "Principles of CMOS VLSI Design" (Weste and Eshraghian, 1985) with 15 hours of lectures dedicated to the subject. In the Digital Electronics Laboratory approximately 20 hours will be spent on the design of simple cells and on getting familiar with basic design tools.

It is estimated that roughly a third of the students will seek the second level of expertise (around 40 per year). The emphasis would be on semicustom design based on gate arrays and on module assemblers. Some attention is to be given to fast technologies, mainly ECL with some awareness of GaAs, due to the needs of Optical Communications.

In the proposal specific courses whose creation was envisaged were:

VLSI System Design - 40 hours lectures, 60 hours laboratories.

The first half of the course will cover Design Methods and System Design Tools. Structured design and Testing are to be emphasised. The second half of the course is to be dedicated to Case Studies.

Students will design a gate array to be part of a board-level system. Complete system testing is envisaged in the second half of the academic year.

VLSI Computer Architecture - 25 hours lectures, 40 hours laboratories.

The course will concentrate on processor design. RISC and Parallel Computer architectures will be covered from a VLSI implementation perspective. In the Lab. students will be using high-level CAD tools for system design (Silicon Compiler) to design simple dedicated processors.

## Project - 220 hours

4 to 6 project groups (8 to 12 students) will do major VLSI design in their final year. A larger number will have to design a gate array as part of their final year project. The department was also planning the launch of an M.Sc. degree and a 22 hour lecture course on VLSI design was included in the syllabus.

Concerning postgraduate research VLSI design facilities were considered essential to projects that the Computer, Biomedical and Optical research groups were starting. They would also be very beneficial to a number of projects already under development. The Bus Interface Logic and the Communications Manager for a Multimicroprocessor System, an Address Processor for an Image Display, the processor for the Pseudo-Star LAN developed within the Computer Networks research group and its node interface logic, Coder and Decoder for 8 and 140 Mbits/s Fiber Optic Digital Transmission, the hardware of DORIS (Dynamic Overlayed Recording of Imaging and Signalling), are cases of well advanced projects where VLSI would be very beneficial.

It was forecast that once facilities became available and self expertise builds up the number of research projects with a VLSI content would rapidly increase.

The department clearly lacked the human resources necessary to implement this program, even if a major effort would be made to improve the VLSI knowledge of existing staff. Hence, apart from workstations and software and a tester, it was requested that the VLSI Design Action would pay for the installation of a lecturer post at Aveiro. Plans were also laid out to get the collaboration of the Microelectronics Group of the Department of Electrical Engineering and Electronics at UMIST for teaching VLSI at Aveiro. This was to be done within an ERASMUS project where both institutions were partners, together with University of Bristol and Universidade do Minho.

### 3.2. The Implementation

The running of the VLSI Design Action was awarded to a consortium of 5 institutions that was to be named EUROCHIP. Our proposal was successful and Universidade de Aveiro became a Participating Institution (PI) in EUROCHIP. The installation of a lecturer post during 2 years and a workstation were to be paid for by EUROCHIP.

Concerning the main design packages on offer, Cadence and Mentor, the former was adopted. This was in fact a choice common to all Portuguese universities participating in EUROCHIP. HSPICE and System HILO were included. A single seat licence for Mentor was bought, since it was considered useful to experiment with another set of tools, and in particular with Genesil and GDT that were part of the Mentor suite.

The delivery of software has been quite slow. Cadence was received during Christmas 1990, together with HILO and HSPICE. Mentor was only delivered in February 1992.

To fill the lecturer post the university was looking for someone from abroad, due to the lack of available know-how in Portugal. The job was widely advertised and personal contacts were made. After some difficulty in finding suitable candidates the post was filled in March 1991 by someone with considerable VLSI design experience.

As a result of these delays the first course on VLSI design only took place in the 2nd semester of 1990-91. It was a 30 hour lecture course given by UMIST staff, with 40

an we we

We .

ā

hours of laboratory sessions, attended by 16 students. In the academic year 1991-92 four courses are being offered, both as final year and M.Sc. courses, one of which lectured by UMIST staff. The courses lectured by our own staff are *VLSI System Design, VLSI Architectures* and *Analog VLSI Design*. A major project, the design of a 32-bit RISC processor was completed as part of the *VLSI Architectures* course, using Cadence (Marriott and Ferrari, 1992) and has just been submitted for fabrication.

A significant effort has been made by the staff to acquire expertise in VLSI design. So far 5 members of staff have attended courses on VLSI offered within the EUROCHIP initiative. Comparing what has happened so far with the plans laid out in the original proposal, there are some discrepancies worth mentioning:

- 1. A 2-phase strategy for the introduction of VLSI into the curriculum developed. In the first phase, being implemented in the present academic year, 1991-92, the basic curriculum remained unchanged, VLSI courses being offered as optional subjects. In the second phase, probably to be implemented from 1992-3, VLSI topics will filter through to the basic courses, as a result of some major curriculum changes presently being discussed.
- 2. Given the lack of support for gate array based design within EUROCHIP, the plans to make gate arrays an important topic in the curriculum were abandoned.
- 3. Analog VLSI is taking a more prominent role than was originally envisaged due to the interest of the staff in charge of the existing courses on Analog Electronics

In what regards research students the late availability of the design tools delayed their use, that was further impaired by a shortage of workstations to run the CAD packages. A significant effort is however being made by the various research groups to equip themselves for VLSI design, and some research designs have already started. A requirement for GaAs has arisen from the Optical and Microwave Communications groups and a case is being made to EUROCHIP in order to get the Plessey F20 library.

ware to constance.

S DAUD - 100 and inc.

# 4. Conclusions

EUROCHIP participation has allowed a department with minimal expertise in VLSI design to embark on a major restructuring of the program of studies offered to its students and enlarge its research activities. Critical to what has been achieved so far has been a strong commitment from the existing staff, the creation of staff posts in VLSI design and collaboration with other universities both under European programs such as ERASMUS and under national initiatives.

#### References

Marriott A.P. and Ferrari A.B. (1992): ARICH experience in teaching VLSI Design and Computer Architecture.- Submitted to: Third EUROCHIP Workshop on VLSI Design Training, Grenoble, France.

Weste N. and Eshraghian K. (1985): Principles of CMOS VLSI Design. Addison-Wesley.

36